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	[Abstract] [PDF	Full-Text (272 KB)]	IEEE CNF					
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# 5 Automated transistor sizing algorithm for minimizing spurious switc activities in CMOS circuits

Wroblewski, A.; Schimpfle, C.V.; Nossek, J.A.; Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on , Volume: 3 , 28-31 May 2000 Pages: 291 - 294 vol.3

[Abstract] [PDF Full-Text (328 KB)] IEEE CNF

# 6 Modeling and layout optimization of VLSI devices and interconnects deep submicron design

Cong, J.;

Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia a South Pacific , 28-31 Jan. 1997

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[Abstract] [PDF Full-Text (748 KB)] IEEE CNF

### 7 Experiments with a performance driven module generator

Kim, S.; Owens, R.M.; Irwin, M.J.;

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